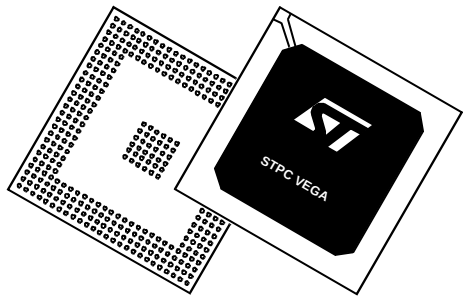
STPC VEGA

X86 CORE PC COMPATIBLE SOC with ETHERNET and USB

PRODUCT PREVIEW

- PENTIUM® II CLASS PROCESSOR UP TO 250 MHZ
- 64-BIT SDRAM CONTROLLER RUNNING AT UP TO 100 MHZ
- PCI 2.2 COMPLIANT MASTER/SLAVE CONTROLLER
- ISA MASTER / SLAVE
- DUAL PORT USB HOST CONTROLLER (OCHI)
- 10/100 ETHERNET MAC
- INTEGRATED PERIPHERAL CONTROLLER WITH SUPPPORT FOR EXTERNAL RTC
- ULTRA DMA-66 IDE CONTROLLER
- POWER MANAGEMENT UNIT
- 16-BIT LOCAL BUS INTERFACE
- I2C BUS CONTROLLER
- UART (1 RxTx)
- IEEE 1149.1 JTAG INTERFACE
- Eight GENERAL PURPOSE IO
- PROGRAMMABLE CLOCKS
- 0.18 MICRON TECHNOLOGY.
- 1.8 V CORE & 3.3 V I/O'S
- MAXIMUM POWER DISSIPATION; 3.1 W @ 250 MHZ

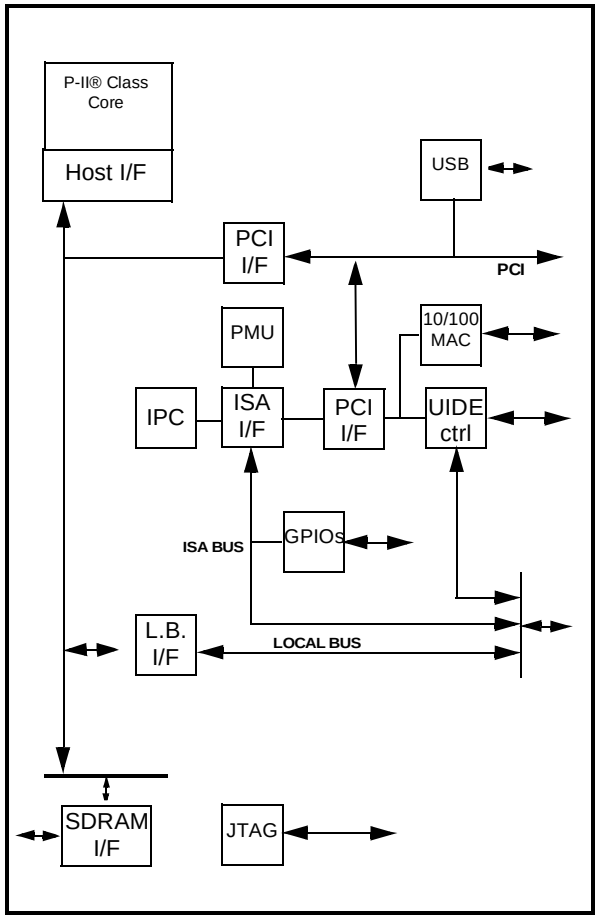


PBGA388

DESCRIPTION

The STPC VEGA integrates a fully static Pentium® II® Class processor, fully compatible with Industry Standards, and combines it with a powerful chipset to provide a general purpose PC compatible subsystem on a single device. The device is packaged in a 388 Ball Grid Array (PBGA).

Logic Diagram



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- **X86 Processor**
- x86 Pentium® II class compatible processor running up to 133MHz in X1 mode and up to 250MHz in X2 mode
  -3 Issue integer 6 stage pipeline/clock
  -3 issue MMX®/clock
  -Pipelined FPU
- Bus clock with skew correction
- Internal core clocks generated as multiples of bus clock with multiplication factors of X1, X2, X2.5, X3, X3.5

- **SDRAM Interface**
- 64-bit data bus
- 100 MHz maximum SDRAM clock
- 8 MByte to 256 MByte memory size
- Supports 16 Mbit, 64 Mbit, 128 Mbit and 256 Mbit memories
- Support of -8, -10, -12, -13, -15 memory parts
- Supports Buffered, non-buffered & registered DIMMs
- Programmable latency

- **PCI Controller Master/Slave**
- Fully compliant with PCI Version 2.2 specification
- Integrated PCI arbitration interface. Up to three external masters can directly connected
- Master/Slave Bridge to USB, LAN, UIDE & ISA cycles
- Support for burst read/write from PCI master
- 0.20X, 0.25X, 0.33X and 0.5X Host clock PCI clock.

- **ISA Master/Slave**
- Generates the ISA clock from either 14.318 MHz oscillator clock or PCI clock
- Supports programmable extra wait state for ISA cycles
- Supports I/O recovery time for back to back I/O cycles
- Fast Gate A20 and Fast reset
- Supports Flash ROM
- Supports ISA hidden refresh
- Buffered DMA and ISA master cycles to reduce the bandwidth utilization of PCI and system bus

- **Local Bus**
- Multiplxed with ISA interface
- 16-bit bus data path with word steering capability
- Two cacheable banks of 16 Mbyte flash devices (boot block shadowed to 000F0000h)
- Programmable timing with host clock granularity for flash accesses
- 32-bit flash burst support
- Two-level hardware key protection for flash boot block protection
- Up to four IO devices supported with programmable start address & size
- IO device timing (setup & recovery time) programmable
- No interrupt support

- **Integrated Peripherals Controller**
- Interrupt Controller: 8259 compatible (two Interrupt controllers)
- DMA Controller: 8237 compatible (two DMA controllers)
- Page register
- Counter 0 and counter 1 gates are always on, counter 2 is controlled by writing to Port B
- Supports external RTC

- **Ultra DMA-66 IDE Controller**
- Supports UIDE hard drives larger than 528 MB
- Support for two connectors to allow up to four drives
- Support for CD-ROM and tape peripherals
- Support for 11.1/16.6 Mbytes/second, I/O Channel Ready PIO data transfers
- Supports up to 66 Mbytes/second, UDMA data transfers
- Ultra DMA supports CRC-16 error checking protocol (no correction supported)
- Support for PIO mode 3 & 4 and DMA mode 1 & 2
- Backward compatibility with IDE (ATA-1)

- **GPIO**
- Individual pins programmable as either input or output
- Interupt generation with selectable masking

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- **USB Host Controller**
- Open HCI Rev 1.1 compatible
- USB Rev 1.1 compatible
- Root hub with two down-stream ports with power switching control
- Support of both low & high speed USB devices
- Support of system management interupt (SMI)

- **10/100 Ethernet Controller**
- Compliant with IEEE 802.3, 802.3u specification
- Supports 10/100 Mb/s data transfer rates
- IEEE 802.3 compliant MII interface to talk to an external PHY
- VLAN support
- Supports both full-duplex and half-duplex operations
- Support of CSMA/CD Protocol for half-duplex
- Supports flow-control for full-duplex operation
- Collision detection and auto retransmission on collisions in half-duplex mode
- Management support by using variety of counters
- Preamble generation and removal
- Automatic 32-bit CRC generation and checking
- Options to insert PAD/CRC32 on transmit
- Options for Automatic Pad stripping on the receive packets
- Provides External and internal loop back capability on the MII Interface
- Contains a variety of flexible address filtering modes on the Ethernet side: - One 48-bit Perfect address - 64 hash-filtered multicast addresses - Pass all multicast addresses - Promiscuous Mode - Pass all incoming packets with a status report

- **UARTs**
- One UART RxTx only
- Programmable word length, stop bits and parity
- Programmable baud rate generator
- Interrupt generator
- Loop-back mode
- Scratch register
- Two 16-byte FIFOs

- **Power Management Unit**
- Four power saving modes: On, Doze, Standby, Suspend
- Programmable system activity detector
- Supports Intel & Cyrix SMI & SMM
- Supports STPCLK#

- **I2C Bus Controller**
- One I2C compliant master/slave bus controller

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